

## IN THE CLAIMS:

Please enter the following claim set:

1. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;
- a gate electrode formed on the gate dielectric film; and
- a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

- a thickness of the SOI film is 0.084  $\mu\text{m}$  or greater and 0.094  $\mu\text{m}$  or smaller, and an

B' impurity concentration of the SOI film is  $7.95 \times 10^{17}/\text{cm}^3$  or greater and  $8.05 \times 10^{17}/\text{cm}^3$  or smaller.

2. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;
- a gate electrode formed on the gate dielectric film; and
- a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,

wherein, when a power supply voltage of 0.6 V is used,

- a thickness of the SOI film is 0.089  $\mu\text{m}$  or greater and 0.099  $\mu\text{m}$  or smaller, and an

impurity concentration of the SOI film is  $8.95 \times 10^{17}/\text{cm}^3$  or greater and  $9.05 \times 10^{17}/\text{cm}^3$  or smaller.

3. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;
- a gate electrode formed on the gate dielectric film; and
- a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used,
- a thickness of the SOI film is 0.093  $\mu\text{m}$  or greater and 0.103  $\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $0.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.005 \times 10^{18}/\text{cm}^3$  or smaller.

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4. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;
- a gate electrode formed on the gate dielectric film; and
- a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of 0.6 V is used,
- a thickness of the SOI film is 0.096  $\mu\text{m}$  or greater and 0.106  $\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $1.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.105 \times 10^{18}/\text{cm}^3$  or smaller.

5. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and  
 a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,  
 wherein, when a power supply voltage of 0.6 V is used,  
 a thickness of the SOI film is 0.100  $\mu\text{m}$  or greater and 0.110  $\mu\text{m}$  or smaller, and an  
 impurity concentration of the SOI film is  $1.195 \times 10^{18}/\text{cm}^3$  or greater and  $1.205 \times 10^{18}/\text{cm}^3$  or  
 smaller.

6. (original) A semiconductor device to be used for a CMOS inverter circuit, the  
 semiconductor device comprising:

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a dielectric film formed on a semiconductor substrate;  
 a SOI film comprising single crystal Si formed on the dielectric layer film;  
 a gate dielectric film formed on the SOI film;  
 a gate electrode formed on the gate dielectric film; and  
 a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,  
 wherein, when a power supply voltage of 0.8 V is used,  
 a thickness of the SOI film is 0.068  $\mu\text{m}$  or greater and 0.078  $\mu\text{m}$  or smaller, and an  
 impurity concentration of the SOI film is  $7.95 \times 10^{17}/\text{cm}^3$  or greater and  $8.05 \times 10^{17}/\text{cm}^3$  or  
 smaller.

7. (original) A semiconductor device to be used for a CMOS inverter circuit, the  
 semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;  
 a SOI film comprising single crystal Si formed on the dielectric layer film;  
 a gate dielectric film formed on the SOI film;  
 a gate electrode formed on the gate dielectric film; and  
 a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,  
 wherein, when a power supply voltage of 0.8 V is used,

a thickness of the SOI film is  $0.074\text{ }\mu\text{m}$  or greater and  $0.084\text{ }\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $8.95 \times 10^{17}/\text{cm}^3$  or greater and  $9.05 \times 10^{17}/\text{cm}^3$  or smaller.

8. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of  $0.8\text{ V}$  is used,

a thickness of the SOI film is  $0.078\text{ }\mu\text{m}$  or greater and  $0.088\text{ }\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $0.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.005 \times 10^{18}/\text{cm}^3$  or smaller.

9. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;

a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;

a gate electrode formed on the gate dielectric film; and

a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of  $0.8\text{ V}$  is used,

a thickness of the SOI film is  $0.083\text{ }\mu\text{m}$  or greater and  $0.093\text{ }\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $1.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.105 \times 10^{18}/\text{cm}^3$  or smaller.

10. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;
- a gate electrode formed on the gate dielectric film; and
- a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of  $0.8 \text{ V}$  is used, a thickness of the SOI film is  $0.087 \text{ }\mu\text{m}$  or greater and  $0.097 \text{ }\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $1.195 \times 10^{18}/\text{cm}^3$  or greater and  $1.205 \times 10^{18}/\text{cm}^3$  or smaller.

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11. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;
- a gate dielectric film formed on the SOI film;
- a gate electrode formed on the gate dielectric film; and
- a diffusion layer for source/drain regions formed in source/drain regions of the SOI film, wherein, when a power supply voltage of  $1.0 \text{ V}$  is used, a thickness of the SOI film is  $0.057 \text{ }\mu\text{m}$  or greater and  $0.067 \text{ }\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $7.95 \times 10^{17}/\text{cm}^3$  or greater and  $8.05 \times 10^{17}/\text{cm}^3$  or smaller.

12. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
- a SOI film comprising single crystal Si formed on the dielectric layer film;

a gate dielectric film formed on the SOI film;  
 a gate electrode formed on the gate dielectric film; and  
 a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,  
 wherein, when a power supply voltage of 1.0 V is used,  
 a thickness of the SOI film is 0.063  $\mu\text{m}$  or greater and 0.073  $\mu\text{m}$  or smaller, and an  
 impurity concentration of the SOI film is  $8.95 \times 10^{17}/\text{cm}^3$  or greater and  $9.05 \times 10^{17}/\text{cm}^3$  or  
 smaller.

13. (original) A semiconductor device to be used for a CMOS inverter circuit, the  
 semiconductor device comprising:

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a dielectric film formed on a semiconductor substrate;  
 a SOI film comprising single crystal Si formed on the dielectric layer film;  
 a gate dielectric film formed on the SOI film;  
 a gate electrode formed on the gate dielectric film; and  
 a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,  
 wherein, when a power supply voltage of 1.0 V is used,  
 a thickness of the SOI film is 0.068  $\mu\text{m}$  or greater and 0.078  $\mu\text{m}$  or smaller, and an  
 impurity concentration of the SOI film is  $0.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.005 \times 10^{18}/\text{cm}^3$  or  
 smaller.

14. (original) A semiconductor device to be used for a CMOS inverter circuit, the  
 semiconductor device comprising:

a dielectric film formed on a semiconductor substrate;  
 a SOI film comprising single crystal Si formed on the dielectric layer film;  
 a gate dielectric film formed on the SOI film;  
 a gate electrode formed on the gate dielectric film; and  
 a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,  
 wherein, when a power supply voltage of 1.0 V is used,

a thickness of the SOI film is 0.072  $\mu\text{m}$  or greater and 0.082  $\mu\text{m}$  or smaller, and an impurity concentration of the SOI film is  $1.095 \times 10^{18}/\text{cm}^3$  or greater and  $1.105 \times 10^{18}/\text{cm}^3$  or smaller.

15. (original) A semiconductor device to be used for a CMOS inverter circuit, the semiconductor device comprising:

- a dielectric film formed on a semiconductor substrate;
  - a SOI film comprising single crystal Si formed on the dielectric layer film;
  - a gate dielectric film formed on the SOI film;
  - a gate electrode formed on the gate dielectric film; and
  - a diffusion layer for source/drain regions formed in source/drain regions of the SOI film,
- wherein, when a power supply voltage of 1.0 V is used,
- a thickness of the SOI film is 0.076  $\mu\text{m}$  or greater and 0.086  $\mu\text{m}$  or smaller, and an

impurity concentration of the SOI film is  $1.195 \times 10^{18}/\text{cm}^3$  or greater and  $1.205 \times 10^{18}/\text{cm}^3$  or smaller.

16. (new) A semiconductor device as in claim 1, further comprising first and second low concentration diffusion regions in contact with source/drain regions, the first and second low concentration diffusion regions having a lower impurity concentration than the source/drain regions, wherein a portion of each of the low concentration diffusion regions extends under the gate electrode.